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This listing of claims will replace all prior versions, and listings, of claims in the application:

## Claim 1 (canceled)

Claim 2 (currently amended): An apparatus for processing a 1 signal used to communicate a block of data representing at <u>least one symbol</u>, the apparatus comprising: 3 a Fourier transform circuit for performing at least 4 one Fourier transform on a said signal used to communicate 5 a block of data representing at least one symbol; a buffer coupled to said Fourier transform circuit for 7 buffering data produced from an output of said Fourier 8 transform circuit; a jitter compensation filter coupled to said buffer 10 for performing a filtering operation on data obtained from 11 said buffer corresponding to said block of data to generate 12 a filtered block of data, the jitter compensation filter 13 having an update input for receiving a filter coefficient 14 update signal; 15 an error calculation module coupled to the update 16 input of the jitter compensation filter, the error 17 compensation calculation module generating the filter 18 coefficient update signal from at least one signal error 19 estimate made from the filtered block of data output by the 20 ditter compensation filter; and 21 a control circuit coupled to said error 22 calculation module for determining as a function of said at 23

least one signal error estimate, when to output said

filtered block of data.

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  1 Claim / (previously presented): The apparatus of claim // /,
- 2 further comprising:
- a channel compensation circuit for receiving said
- 4 block of data and performing a channel compensation
- 5 operation on at least a portion of said block of data prior
- 6 to the block of data being stored in said buffer for
- 7 processing by said jitter compensation filter.
- 1 Claim # (original): The apparatus of claim 2, wherein said
- 2 block of data represents a plurality of symbols, the
- 3 apparatus further comprising:
- 4 demodulator circuitry coupled to an output of the
- 5 jitter compensation filter.
- 1 Claim % (previously presented): The apparatus of claim %,
- 2 wherein the error calculation module includes:
- 3 means for generating a decision directed error
- 4 value.
- 1 Claim & (currently amended): An apparatus for processing a
- 2 signal used to communicate a block of data representing at
- 3 least one symbol, the apparatus comprising:
- a Fourier transform circuit for performing at least
- 5 one Fourier transform on a said signal used to communicate
- 6 a block of data representing at least one symbol;
- 7 a buffer coupled to said Fourier transform circuit for
- 8 buffering data produced from an output of said Fourier
- 9 transform circuit;
- a jitter compensation filter coupled to said buffer
- 11 for performing a filtering operation on data obtained from
- 12 said buffer corresponding to said block of data to generate
- 13 a filtered block of data, the jitter compensation filter

14	having an update input for receiving a filter coefficient
15	update signal; and
16	an error calculation module coupled to the update
17	input of the jitter compensation filter, the error
18	compensation calculation module generating the filter
19	coefficient update signal from at least one signal error
20	estimate made from the filtered block of data output by the
21	jitter compensation filter, wherein the error calculation
22	module includes:
23	means for generating a decision directed
24	error value;
25	means for generating a pilot directed error
26	value; and
27	a selection device for selecting one of the
28	decision directed error value and the pilot
29	directed error value to be output.
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1	Claim / (currently amended): An apparatus for processing a
2	signal used to communicate a block of data representing at
3	least one symbol, the apparatus comprising:
4	a Fourier transform circuit for performing at least
5	one Fourier transform on a said signal used to communicate
6	a block of data representing at least one symbol;
7	a buffer coupled to said Fourier transform circuit for
8	buffering data produced from an output of said Fourier
9	transform circuit;
10	a jitter compensation filter coupled to said buffer
11	for performing a filtering operation on data obtained from
12	said buffer corresponding to said block of data to generate
13	a filtered block of data, the jitter compensation filter
14	having an update input for receiving a filter coefficient
15	update signal; and

16	an error calculation module coupled to the update
17	input of the jitter compensation filter, the error
18	compensation calculation module generating the filter
19	coefficient update signal from at least one signal error
20	estimate made from the filtered block of data output by the
21	jitter compensation filter, wherein the error calculation
22	module includes:
23	means for generating a decision directed
24	error value;
25	means for generating a non-decision directed
26	error value; and
27	a selection device for selecting one of the
28	decision directed error value and the non-
29	decision directed error value to be output.
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1	Claim $8$ (previously presented): The apparatus of claim $7$ ,
2	further comprising:
3	an input buffer coupled to the jitter
4	compensation filter for storing said block of data while it
5	being processed multiple times by said jitter compensation
6	filter.
	Claims 9 and 10 (canceled)
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1	Claim // (currently amended): An apparatus for processing
2	a signal used to communicate a block of data representing
3	at least one symbol, the apparatus comprising:
4	a Fourier transform circuit for performing at least

5 one Fourier transform on a said signal used to communicate

6 a block of data representing at least one symbol;

- 7 a buffer coupled to said Fourier transform circuit for
- 8 buffering data produced from an output of said Fourier
- 9 transform circuit;
- a jitter compensation filter coupled to said buffer
- 11 for performing a filtering operation on data obtained from
- 12 said buffer corresponding to said block of data to generate
- 13 a filtered block of data, the jitter compensation filter
- 14 having an update input for receiving a filter coefficient
- 15 update signal, said buffer storing said block of data while
- 16 said block of data is processed multiple times by said
- 17 jitter compensation filter;
- 18 an error calculation module coupled to the update
- 19 input of the jitter compensation filter, the error
- 20 compensation calculation module generating the filter
- 21 coefficient update signal from at least one signal error
- 22 estimate made from the filtered block of data output by the
- 23 jitter compensation filter; and
- 24 an output control device for determining when to
- 25 output the filtered block of data generated by said jitter
- 26 compensation filter.
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    1 Claim 1/2 (original): The apparatus of claim 1/1, wherein
  - 2 the output control device includes:
  - means for determining when said block of data has been
  - 4 filtered a fixed number of times by the jitter compensation
- 5 filter.
- 1 Claim 1/3 (original): The apparatus of claim 1/1,
- wherein the output control device includes an input
- 3 for receiving the filter coefficient update signal
- 4 generated by said error calculation module; and

- 5 wherein the jitter compensation filter further
- 6 includes means for resetting filter coefficient values to a
- 7 set of initial values in response to a reset signal
- 8 generated by said output control device.

## Claims 14 and 15 (canceled)

- Claim 16 (previously presented): A system for processing a
- 2 multi-tone signal, the system including:
- 3 a Fourier transform circuit for performing at least
- one Fourier transform on said multi-tone signal;
- a channel compensation module coupled to said Fourier
- 6 transform circuit for performing a channel compensation
- 7 operation on said multi-tone signal after processing by
- 8 said Fourier transform circuit;
- 9 a buffer coupled to said Fourier transform circuit for
- 10 buffering the channel compensated multi-tone signal;
- a jitter compensation module coupled to said buffer
- 12 for performing a jitter reduction operation on the buffered
- 13 channel compensated multi-tone signal, wherein the jitter
- 14 compensation module includes: a jitter compensation filter
- 15 with programmable filter tap weights, and means for
- 16 iteratively updating the filter tap weights as a function
- 17 of the jitter compensation filter output; and
- a control circuit for determining when the output of
- 19 the jitter compensation filter should be used as the output
- 20 of the jitter compensation module.
- 1 Claim 17 (previously presented): The system of claim 16,
- 2 wherein the means for iteratively updating the filter tap
- 3 weights includes:

a signal error estimation circuit for generating from 4 the output of the jitter compensation filter a measure of a 5 symbol error. Claim 18 (previously presented): A system for processing a 1 multi-tone signal, the system including: 2 a Fourier transform circuit for performing at least 3 one Fourier transform on said multi-tone signal; a channel compensation module coupled to said Fourier 5 transform circuit for performing a channel compensation 6 operation on said multi-tone signal after processing by said Fourier transform circuit; 8 a buffer coupled to said Fourier transform circuit for 9 buffering the channel compensated multi-tone signal; 10 a jitter compensation module coupled to said buffer 11 for performing a jitter reduction operation on the buffered 12 channel compensated multi-tone signal, wherein the jitter 13 compensation module includes : a jitter compensation filter 14 with programmable filter tap weights, and means for 15 iteratively updating the filter tap weights as a function 16 of the jitter compensation filter output, wherein the means 17 for iteratively updating the filter tap weights includes a 18 signal error estimation circuit for generating from the 19 output of the jitter compensation filter a measure of a 20 symbol error; and 21 means for resetting the jitter compensation filter tap 22 weights to an initial set of values in response to the 23 control circuit determining that the output of the jitter 24 compensation filter should be used as the output of the 25

jitter compensation filter.

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1	Claim 19 (previously presented): A method of processing a
2	multi-tone signal, the method comprising the steps of:
3	performing a Fourier transform operation on the multi-
4	tone signal;
5	buffering a block of samples produced from the output
6	of said Fourier transform operation; and
7	performing a jitter compensation operation, said
8	jitter compensation operation including:
9	<ul><li>i) operating a filter having a plurality of tap</li></ul>
10	weights to filter said block of samples to produce a
11	filtered block of data;
12	ii) determining a signal error from the filtered
13	block of data;
14	iii) updating at least one of said plurality of
15	tap weights in said filter as a function of the
16	determined signal error; and
17	iv) repeating steps i, ii, and iii until a filter
18	updating stop criterion is satisfied.
	15°
1	Claim 20 (original): The method of claim 19, further
2	comprising the step of:
3	supplying the filtered block of data output by
4	said filter when said filter updating criterion is
5	satisfied to subsequent receiver circuitry.
	(b),
1	Claim 21 (original): The method of claim 19, wherein said
2	filter updating stop criterion is the completion of a fixed
3	number of filtering operations on said block of data.
	υ <b>7</b>
1	Claim 22 (original): The method of claim 21, wherein said
2	filter updating criterion is a failure in the signal error

3 to exhibit an improvement over the previous signal error.

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  1 Claim 23 (original): The method of claim 29, wherein said
- 2 step of determining a signal error includes generating a
- 3 decision directed error value.
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  1 Claim 24 (original): The method of claim 19, wherein said
- 2 step of determining a signal error includes generating a
- 3 non-decision directed error value.
- 1 Claim 25 (previously presented): The method of claim 19,
- 2 further comprising:
- 3 prior to performing said buffering, performing a
- 4 channel compensation operation on said block of data.
- 1 Claim 26 (original): The method of claim 25, a single
- 2 channel compensation operation is performed on the block of
- 3 data in a first period of time; and
- 4 step i, ii and iii are performed multiple times
- 5 in a time period which is equal to or shorter than the
- 6 first time period.